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1 MemorIES3: a programmable, real-time hardware emulation tool for multiprocessor server design
Ashwini Nanda, Kwok-Ken Mak, Krishnan Sugarvanam, Ramendra K. Sahoo, Vijayaraghavan Soundarararjan, T. Basil Smith
November 2000 **Proceedings of the ninth international conference on Architectural support for programming languages and operating systems**, Volume 34 , 28 Issue 5 , 5

Full text available: 📄 pdf(724.53 KB)   Additional Information: full citation, abstract, references, citings, index terms

Modern system design often requires multiple levels of simulation for design validation and performance debugging. However, while machines have gotten faster, and simulators have become more detailed, simulation speeds have not tracked machine speeds, As a result, it is difficult to simulate realistic problem sizes and hardware configurations for a target machine. Instead, researchers have focussed on developing sealing methodologies and running smaller problem sizes and configurations that atte ...

2 MemorIES: a programmable, real-time hardware emulation tool for multiprocessor server design
Ashwini Nanda, Kwok-Ken Mak, Krishnan Sugavanam, Ramendra K. Sahoo, Vijayaraghavan Soundararajan, T. Basil Smith
November 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 11

Full text available: 📄 pdf(1.84 MB)   Additional Information: full citation, abstract, references, index terms

Modern system design often requires multiple levels of simulation for design validation and performance debugging. However, while machines have gotten faster, and simulators have become more detailed, simulation speeds have not tracked machine speeds. As a result, it is difficult to simulate realistic problem sizes and hardware configurations for a target machine. Instead, researchers have focussed on developing scaling methodologies and running smaller problem sizes and configurations that atte ...

3 FPGA-based systems: An SoC design methodology using FPGAs and embedded microprocessors
Nobuyuki Ohba, Kohji Takano
June 2004 **Proceedings of the 41st annual conference on Design automation - Volume 00**

Full text available: 📄 pdf(75.56 KB)   Additional Information: full citation, abstract, references, index terms

In System on Chip (SoC) design, growing design complexity has forced designers to start designs at higher abstraction levels. This paper proposes an SoC design methodology that makes full use of FPGA capabilities. Design modules in different abstraction levels are all combined and run together in an FPGA prototyping system that fully emulates the target SoC. The higher abstraction level design modules run on microprocessors embedded in the FPGAs, while lower-level synthesizable RTL design module ...

Keywords: ASIC, FPGA prototyping, SoC, mixed-level verification

4   The Transmogrifier-2: a 1 million gate rapid prototyping system
David M. Lewis, David R. Galloway, Marcus van Ierssel, Jonathan Rose, Paul. Chow
February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-
        programmable gate arrays**
Full text available: pdf(1.31 MB)   Additional Information: full citation, references, citings, index terms

5   Rapid prototyping of ASIC based systems
P. H. Kelly, K. J. Page, P. M. Chau
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(139.19 KB)   Additional Information: full citation, references, index terms

6   Exploiting FPGA-features during the emulation of a fast reactive embedded system
Karlheinz Weiß, Thorsten Steckstor, Gernot Koch, Wolfgang Rosenstiel
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium
        on Field programmable gate arrays**
Full text available: pdf(2.02 MB)   Additional Information: full citation, references, citings, index terms

7   Board-level multiterminal net routing for FPGA-based logic emulation
Wai-Kei Mak, D. F. Wong
April 1997 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
        Volume 2 Issue 2
Full text available: pdf(376.05 KB)   Additional Information: full citation, abstract, references, citings, index
                                                                       terms, review

We consider a board-level routing problem applicable to FPGA-based logic emulation systems such as the Realizer System [Varghese et al. 1993] and the Enterprise Emulation System [Maliniak 1992] manufactured by Quickturn Design Systems. Optimal algorithms have been proposed for the case where all nets are two-terminal nets [Chan and Schlag 1993; Mak and Wong 1995]. We show how multiterminal nets can be handled by decomposition into two-terminal nets. We show that the multiterminal net decomp ...

Keywords: board-level routing, crossbars, field programmable gate arrays, logic emulation, multi-terminal net decomposition

8   The design of RPM: an FPGA-based multiprocessor emulator
Koray Öner, Luiz A. Barroso, Sasan Iman, Jaeheon Jeong, Krishnan Ramamurthy, Michel Dubois
February 1995 **Proceedings of the 1995 ACM third international symposium on Field-
        programmable gate arrays**

Full text available: pdf(54.01 KB)   Additional Information: full citation, abstract, references, citings, index terms

Recent advances in Field-Programmable Gate Arrays (FPGA) and programmable interconnects have made it possible to build efficient hardware emulation engines. In addition, improvements in Computer-Aided Design (CAD) tools, mainly in synthesis tools, greatly simplify the design of large circuits. The RPM (Rapid Prototype Engine for Multiprocessors) Project leverages these two technological advances. Its goal is to develop a common hardware platform for th ...

Keywords: field-programmable gate arrays, logic emulation, message-passing multicomputers, rapid prototyping, shared-memory multiprocessors

9 Wormhole IP over (connectionless) ATM
Manolis G. H. Katevenis, Iakovos Mavroidis, Georgios Sapountzis, Eva Kalyvianaki, Ioannis Mavroidis, Georgios Glykopoulos
October 2001 **IEEE/ACM Transactions on Networking (TON)**, Volume 9 Issue 5

Full text available: pdf(211.25 KB)   Additional Information: full citation, abstract, references, citings, index terms

High-speed switches and routers internally operate using fixed-size cells or segments; variable-size packets are segmented and later reassembled. Connectionless ATM was proposed to quickly carry IP packets segmented into cells (AAL5) using a number of hardware-managed ATM VCs. We show that this is analogous to wormhole routing. We modify this architecture to make it applicable to existing ATM equipment: we propose a low-cost, single-input, single-output Wormhole IP Router that functions as a VP/ ...

Keywords: Connectionless ATM, IP over ATM, gigabit router, routing filter, wormhole IP, wormhole routing

10 On optimal board-level routing for FPGA-based logic emulation
Wai-Kei Mak, D. F. Wong
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(200.79 KB)   Additional Information: full citation, references, citings, index terms

11 Board-level multi-terminal net routing for FPGA-based logic emulation
Wai-Kei Mak, D. F. Wong
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(221.26 KB)   Additional Information: full citation, abstract, references, citings, index terms
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We consider a board-level routing problem applicable to FPGA-based logic emulation systems such as the Realizer System [3] and the Enterprise Emulation System [5] manufactured by Quickturn Systems. Optimal algorithms have been proposed for the case where all nets are two-terminal nets [10,11]. In this paper, we show how multi-terminal nets can be handled by decomposition into two-terminal nets. We show that the multi-terminal net decomposition problem can be modelled as a bounded-degree hypergra ...

Keywords: board-level routing, bounded-degree hypergraph-to-graph transformation, FPGA, logic emulation systems, multi-terminal net decomposition net

12 Prototyping, verification, and test: Implementation of BEE: a real-time large-scale hardware emulation engine

Chen Chang, Kimmo Kuusilinna, Brian Richards, Robert W. Brodersen

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(3.65 MB)   Additional Information: full citation, abstract, references, index terms

> This paper describes the hardware implementation of a real-time, large-scale, multi-chip FPGA (Field Programmable Gate Array) based emulation engine with a capacity of 10 million ASIC (Application Specific Integrated Circuits) equivalent gates. Attainable system operation frequency can exceed 60 MHz, and the system throughput has been empirically verified to achieve 600 billion 16-bit additions per second. The emulator is custom designed to maximize the performance and resource utilization for a ...
>
> **Keywords**: FPGA, hardware emulation, rapid-prototyping

13 Module generation of complex macros for logic-emulation applications

Wen-Jong Fang, Allen C.-H. Wu, Duan-Ping Chen

February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**

Full text available: pdf(1.48 MB)   Additional Information: full citation, references, citings, index terms

14 A hybrid complete-graph partial-crossbar routing architecture for multi-FPGA systems

Mohammed A. S. Khalid, Jonathan Rose

March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

Full text available: pdf(1.12 MB)   Additional Information: full citation, abstract, references, citings, index terms

> Multi-FPGA systems (MFSs) are used as custom computing machines, logic emulators and rapid prototyping vehicles. A key aspect of these systems is their programmable routing architecture; the manner in which wires, FPGAs and Field-Programmable Interconnect Devices (FPIDs) are connected. Several routing architectures for MFSs have been proposed [Arno92] [Butt92] [Hauc94] [Apti96] [Vuil96] and previous research has shown that the partial crossbar is one of the best existing architectures [Kim9 ...

15 Reconfigurable systems: SmartGlue: an interface controller with auto reconfiguration for field programmable computing machine

Young-Il Kim, Bong-Il Park, Jae-Gon Lee, Chong-Min Kyung

January 2004

Full text available: pdf(113.02 KB)
                       Publisher Site   Additional Information: full citation, abstract, references

> This paper describes an interface controller called SmartGlue which enables a processor to interface with peripherals and makes a system reconfigurable by programming FPGA on the fly. By supporting standard interfaces and plug and play mechanism for the processor and FPGA, one can use any type of processors and FPGA's to implement a field programmable computing machine. The performance and utility of the SmartGlue was validated by applying its silicon implementation into a real system.

16 Software for Reconfigurable Systems: Incremental reconfiguration of multi-FPGA systems

K. K. Lee, D. F. Wong

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: 📄 pdf(146.68 KB)   Additional Information: full citation, abstract, references

In reconfigurable computing, circuits implemented on multi-FPGA systems have to be incrementally modified. Since reconfiguring an FPGA is time-consuming, the time for reconfiguration depends on the number of FPGAs to be reconfigured. Our objective is to reduce the number of such FPGAs. In this paper, we consider the specific problem of incrementally reconfiguring a multi-FPGA system that utilizes the direct interconnection architecture, where routing connections between FPGAs are to neighbors th ...

17 Poster session 2: A comparison between mask- and field-programmable routing structures on industrial FPGA architectures

Luca Macchiarulo, Consolato F. Caccamo, Davide Pandini
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: 📄 pdf(136.43 KB)   Additional Information: full citation, abstract, references, index terms

In this paper we compare the routing architecture of island-style FPGAs based on field-programmable switch boxes with a mask-programmable routing structure, in order to assess its position in the design space of routing opportunities available to VLSI IC designers. Although the results presented in this work depend on a few implementation details that will be discussed in the paper, the mask-programmable routing structure shows a large area saving and delay improvement with respect to the field- ...

Keywords: FPGA, interconnect architectures, mask-programmable, routing

18 Placement: Hardware-assisted simulated annealing with application for fast FPGA placement

Michael G. Wrighton, André M. DeHon
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: 📄 pdf(503.33 KB)   Additional Information: full citation, abstract, references, citings, index terms

To truly exploit FPGAs for rapid turn-around development and prototyping, placement times must be reduced to seconds; late-bound, reconfigurable computing applications may demand placement times as short as microseconds. In this paper, we show how a systolic structure can accelerate placement by assigning one processing element to each possible location for an FPGA LUT from a design netlist. We demonstrate that our technique approaches the same quality point as traditional simulated annealing as ...

Keywords: design automation, field-programmable gate arrays, placement, reconfigurable computing, simulated annealing

19 Multi-terminal net routing for partial crossbar-based multi-FPGA systems

Abdel Ejnioui, N. Ranganathan
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Full text available: 📄 pdf(1.06 MB)   Additional Information: full citation, references, citings, index terms

Keywords: FPGA architecture, FPGA routing, branch-and-price, integer programming, interconnect optimization, layout synthesis

20 Multiway FPGA partitioning by fully exploiting design hierarchy
Wen-Jong Fang, Allen C.-H. Wu
January 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 1

Full text available: pdf(130.36 KB)   Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new integrated synthesis and partitioning method for multiple-FPGA applications. Our approach bridges the gap between HDL synthesis and physical partitioning by fully exploiting the design hierarchy. We propose a novel multiple-FPGA synthesis and partitioning method which is performed in three phases: (1) fine-grained synthesis, (2) functional-based clustering, and (3) hierarchical set-covering partitioning. This method first synthesizes a design specification in ...

Keywords: fine-grained synthesis, functional clustering, multi-way partitioning, multiple-FPGA synthesis

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1 Performance-driven placement for dynamically reconfigurable FPGAs   ▨
Guang-Ming Wu, Jai-Ming Lin, Yao-Wen Chang
October 2002 **ACM Transactions on Design Automation of Electronic Systems
            (TODAES)**, Volume 7 Issue 4
Full text available: 🗎 pdf(221.44 KB)   Additional Information: full citation, abstract, references, index terms

In this article, we introduce a new placement problem motivated by the Dynamically
Reconfigurable FPGA (DRFPGA) architectures. Unlike traditional placement, the problem for
DRFPGAs must consider the precedence constraints among logic components. For the
placement, we develop an effective metric that can consider wirelength, register
requirement, and power consumption simultaneously. With the considerations of the new
metric and the precedence constraints, we then present a three-stage scheme of ...

Keywords: Computer-aided design of VLSI, dynamically reconfigurable, field-
programmable gate array, layout, placement

2 Depth optimal incremental mapping for field programmable gate arrays   ▨
Jason Cong, Hui Huang
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: 🗎 pdf(166.95 KB)   Additional Information: full citation, abstract, references, citings, index
                                                                   terms

In this paper, we study the incremental technology mapping problem for lookup-table (LUT)
based Field Programmable Gate Arrays (FPGAs) under incremental changes. Given a gate-
level networks, a mapping solution associated with it, and a sequence of changes to the
original network, we compute a new mapping solution by modifying the existing one.
Moreover, we assume that the given mapping solution is depth-optimal and we are required
to come up with a modified mapping solution that maintains t ...

3 Tools: Incremental physical resynthesis for timing optimization   ▨
Peter Suaris, Lungtien Liu, Yuzheng Ding, Nanchi Chou
February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on
              Field programmable gate arrays**
Full text available: 🗎 pdf(762.18 KB)   Additional Information: full citation, abstract, references, index terms

This paper presents a new approach to timing optimization for FPGA designs, namely
incremental physical resynthesis, to answer the challenge of effectively integrating logic and
physical optimizations without incurring unmanageable runtime complexity. Unlike previous

approaches to this problem which limit the types of operations and/or architectural features, we take advantage of many architectural characteristics of modern FPGA devices, and utilize many types of optimizations including < ...

Keywords: FPGA, logic synthesis, placement, timing optimization

4 Optimal FPGA module placement with temporal precedence constraints
S. Fekete, E. Köhler, J. Teich
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(185.17 KB)   Additional Information: full citation, references, citings, index terms

5 Generating highly-routable sparse crossbars for PLDs
Guy Lemieux, Paul Leventis, David Lewis
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**

Full text available: pdf(952.31 KB)   Additional Information: full citation, abstract, references, citings, index terms

A method for evaluating and constructing sparse crossbars which are both area efficient and highly routable is presented. The evaluation method uses a network flow algorithm to accurately compute the percentage of random test vectors that can be routed. The construction method attempts to maximize the spread of the switch locations, such that any given subset of input wires can connect to as many output wires as possible. Based on Hall's Theorem, we argue that this increases the likelihood ...

6 Innovative Applications: A dynamically reconfigurable adaptive viterbi decoder
Sriram Swaminathan, Russell Tessier, Dennis Goeckel, Wayne Burleson
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: pdf(235.26 KB)   Additional Information: full citation, abstract, references, citings

The use of error-correcting codes has proven to be an effective way to overcome data corruption in digital communication channels. Although widely-used, the most popular communications decoding algorithm, the Viterbi algorithm, requires an exponential increase in hardware complexity to achieve greater decode accuracy. In this paper, we describe the analysis and implementation of a reduced-complexity decode approach, the adaptive Viterbi algorithm (AVA). Our AVA design is implemented in reconfigu ...

Keywords: FPGA, Viterbi coding, dynamic reconfiguration

7 Compilation techniques for embedded applications: Area-efficient instruction set synthesis for reconfigurable system-on-chip designs
Philip Brisk, Adam Kaplan, Majid Sarrafzadeh
June 2004 **Proceedings of the 41st annual conference on Design automation - Volume 00**

Full text available: pdf(221.62 KB)   Additional Information: full citation, abstract, references, index terms

Silicon compilers are often used in conjunction with Field Programmable Gate Arrays (FPGAs) to deliver flexibility, fast prototyping, and accelerated time-to-market. Many of these compilers produce hardware that is larger than necessary, as they do not allow instructions to share hardware resources. This study presents an efficient heuristic which transforms a set of custom instructions into a single hardware datapath on which they can execute. Our approach is based on the classic problems of fi ...

Keywords: compiler, field-programmable gate array (FPGA), integer linear programming (ILP), resource sharing

8 Optimality and Stability Study of Timing-Driven Placement Algorithms

Jason Cong, Michail Romesis, Min Xie
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(316.85 KB)   Additional Information: full citation, abstract, index terms

This work studies the optimality and stability of timing-drivenplacement algorithms. The contributions of this work include twoparts: 1) We develop an algorithm for generating synthetic examples with known optimal delay for timing driven placement(T-PEKO). The examples generated by our algorithm can closelymatch the characteristics of real circuits. 2) Using these syntheticexamples with known optimal solutions, we studied the optimalityof several timing-driven placement algorithms for FPGAs by c ...

9 Poster session 2: A comparison between mask- and field-programmable routing structures on industrial FPGA architectures

Luca Macchiarulo, Consolato F. Caccamo, Davide Pandini
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(136.43 KB)   Additional Information: full citation, abstract, references, index terms

In this paper we compare the routing architecture of island-style FPGAs based on field-programmable switch boxes with a mask-programmable routing structure, in order to assess its position in the design space of routing opportunities available to VLSI IC designers. Although the results presented in this work depend on a few implementation details that will be discussed in the paper, the mask-programmable routing structure shows a large area saving and delay improvement with respect to the field- ...

Keywords: FPGA, interconnect architectures, mask-programmable, routing

10 New FPGA architectures: Using bus-based connections to improve field-programmable gate array density for implementing datapath circuits

Andy Ye, Jonathan Rose
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**
Full text available: pdf(239.44 KB)   Additional Information: full citation, abstract, references, index terms

As the logic capacity of Field-Programmable Gate Arrays (FPGAs) increases, they are being increasingly used to implement large arithmetic-intensive applications, which often contain a large proportion of datapath circuits. Since datapath circuits usually consist of regularly structured components (called bit-slices) which are connected together by regularly structured signals (called buses), it is possible to utilize datapath regularity in order to achieve significant area savings through FPGA a ...

Keywords: FPGA architecture, area efficiency, datapath regularity, reconfigurable fabric, routing architecture

11 Combinational logic synthesis for LUT based field programmable gate arrays

Jason Cong, Yuzheng Ding
April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES),**
Volume 1 Issue 2

Full text available: pdf(628.91 KB)   Additional Information: full citation, abstract, references, citings, index terms, review

The increasing popularity of the field programmable gate-array (FPGA) technology has generated a great deal of interest in the algorithmic study and tool development for FPGA-specific design automation problems. The most widely used FPGAs are LUT based FPGAs, in which the basic logic element is a K-input one-output lookup-table (LUT) that can implement any Boolean function of up to K variables. This unique feature of the LUT has brought new challenges to lo ...

Keywords: FPGA, area minimization, computer-aided design of VLSI, decomposition, delay minimization, delay modeling, logic optimization, power minimization, programmable logic, routing, simplification, synthesis, system design, technology mapping

12 Security on FPGAs: State-of-the-art implementations and attacks

Thomas Wollinger, Jorge Guajardo, Christof Paar
August 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 3

Full text available: pdf(296.79 KB)   Additional Information: full citation, abstract, references, index terms

In the last decade, it has become apparent that embedded systems are integral parts of our every day lives. The wireless nature of many embedded applications as well as their omnipresence has made the need for security and privacy preserving mechanisms particularly important. Thus, as field programmable gate arrays (FPGAs) become integral parts of embedded systems, it is imperative to consider their security as a whole. This contribution provides a state-of-the-art description of security issues ...

Keywords: Cryptography, FPGA, attacks, cryptographic applications, reconfigurable hardware, reverse engineering, security

13 Architecture analysis and automation: An FPGA architecture with enhanced datapath functionality

Katarzyna Leijten-Nowak, Jef L. van Meerbergen
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(188.86 KB)   Additional Information: full citation, abstract, references, index terms

Although FPGAs are a cost-efficient alternative for both ASICs and general purpose processors, they still result in designs which are more than an order of magnitude more costly and slower than their equivalents implemented in dedicated logic. This efficiency gap makes FPGAs less suitable for high-volume cost-sensitive applications (e.g. embedded systems).We show that the intrinsic cost of traditional general-purpose FPGAs can be reduced if they are designed to target an application domain or a ...

Keywords: DSP, FPGAs, adder inverting property, application-domain tuning, logic block architectures, symmetry

14 Analysis of FPGA/FPIC switch modules

Yao-Wen Chang, Kai Zhu, Guang-Ming Wu, D. F. Wong, C. K. Wong
January 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 1

Full text available: pdf(508.09 KB)   Additional Information: full citation, abstract, references, index terms, review

Switch modules are the most important component of the routing resources in

FPGAs/FPICs. Previous works have shown that switch modules with higher routability result in better area performance for practical applications. We consider in this paper an FPGA/FPIC switch-module analysis problem: the inputs consist of a switch-module description and the number of nets required to be routed through the switch module; the question is to determine if there exists a feasible routing for the routing requir ...

Keywords: Computer-aided design of VLSI, FPGA, FPIC, layout, synthesis

15 Fast placement approaches for FPGAs

Russell Tessier

April 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
Volume 7 Issue 2

Full text available: pdf(606.13 KB)   Additional Information: full citation, abstract, references, index terms

Recent trends in FPGA development indicate a strong shift toward design reuse through the use of intellectual property (IP). This design shift has motivated the development of Frontier, a timing-driven FPGA placement system that uses design macroblocks in conjunction with a series of placement algorithms to achieve highly routable and high-performance layouts quickly. In the first stage of design placement, a macro-based floorplanner is used to quickly identify an initial layout based on interma ...

Keywords: Computer-aided design of VLSI, field-programmable gate arrays, layout, synthesis

16 Applications of reconfigurable computing: Dynamic hardware plugins in an FPGA with partial run-time reconfiguration

Edson L. Horta, John W. Lockwood, David E. Taylor, David Parlour

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(406.97 KB)   Additional Information: full citation, abstract, references, citings, index terms

Tools and a design methodology have been developed to support partial run-time reconfiguration of FPGA logic on the Field Programmable Port Extender. High-speed Internet packet processing circuits on this platform are implemented as Dynamic Hardware Plugin (DHP) modules that fit within a specific region of an FPGA device. The PARBIT tool has been developed to transform and restructure bitfiles created by standard computer aided design tools into partial bitsteams that program DHPs. The methodolo ...

Keywords: FPG, IP, Internet, hardware, modularity, network, packet, partial RTR, platform computing, reconfiguration, routing

17 Reconfigurable computing: analysis and trends: FPGAs vs. CPUs: trends in peak floating-point performance

Keith Underwood

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Full text available: pdf(205.40 KB)   Additional Information: full citation, abstract, references, index terms

Moore's Law states that the number of transistors on a device doubles every two years; however, it is often (mis)quoted based on its impact on CPU performance. This important corollary of Moore's Law states that improved clock frequency plus improved architecture yields a doubling of CPU performance every 18 months. This paper examines the impact of Moore's Law on the peak floating-point performance of FPGAs. Performance trends for individual operations are analyzed as well as the performance tr ...

Keywords: FPGA, floating point, supercomputing, trends

18 General technology mapping for field-programmable gate arrays based on lookup tables
Amit Chowdhary, John P. Hayes
January 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 1
Full text available: pdf(1.07 MB)   Additional Information: full citation, abstract, references, index terms

We present a general technology-mapping methodology (TULIP) for field-programmable gate arrays (FPGAs) that can yield optimal results, and is applicable to any FPGA with a logic block composed of lookup tables (LUTs). We introduce the concept of a virtual switch to model the internal connections of a logic block with multiple LUTs; each configuration of virtual switches is called a multiple-LUT block (MLB). A logic block can be precisely defined by a small but complete set of representative conf ...

Keywords: Basis, circuit partitioning, field-programmable gate arrays, lookup tables (LUTs), mapping, multiple-LUT blocks, nonrooted trees, rooted trees, synthesis

19 Routing: PipeRoute: a pipelining-aware router for FPGAs
Akshay Sharma, Carl Ebeling, Scott Hauck
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Full text available: pdf(179.95 KB)   Additional Information: full citation, abstract, references, citings, index terms

We present a pipelining-aware router for FPGAs. The problem of routing pipelined signals is different from the conventional FPGA routing problem. For example, the two terminal N-Delay pipelined routing problem is to find the lowest cost route between a source and sink that goes through at least N (N > 1) distinct pipelining resources. In the case of a multi-terminal pipelined signal, the problem is to find a Minimum Spanning Tree that contains sufficient pipelining resources such that the del ...

Keywords: BFS, PipeRoute, minimum spanning tree, pipelined circuits, pipelining, routing, retimed circuits, retiming

20 FPGA routing architecture: segmentation and buffering to optimize speed and density
Vaughn Betz, Jonathan Rose
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**
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of a Multiple Neural Network Learning System to **Emulation** of Mortgage Underwriting Judgements, IEEE
the Backpropagation Algorithm Using Reconfigurable **FPGAs** James G. Eldredge and Brad L. Hutchings Dept. of
devoted to it [10]Field Programmable Gate Arrays (**FPGAs**) are an excellent technology for implementing
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A PCI based Network Interface Controller for IEEE.. - Boosten, Dobinson.. (1998) (Correct)
been developed. The board's hardware, controlled by **FPGA** firmware, together with host software, provides a
Pci Based Network Controller For Ieee 1355 Ds Links **Fpga** C101 Amcc Ds Ds C101 Ram Dsnic Pci Figure 1:
The
Altera FLEX 10K50 Field-Programmable Gate Array (**FPGA**)The spare pins of the **FPGA** are brought out to
www.cern.ch/HSI/dshs/publications/wotug21/dsnic/ps/dsnic.ps.gz

Signalling Protocol for P4 (SPP4), version 1.0 - Hadzic (1998) (Correct)
functions of the device driver are managing the **FPGA** devices and handling signalling messages. Device
it. This operation is slow since downloading the **FPGA** device is a lengthy process. If the free device
sends the signalling message ffl P4RDPE reads the **FPGA** device status ffl P4RMPE removes the processing
www.cis.upenn.edu/~boosters/SPP4.ps

Building the 4 Processor SB-PRAM Prototype - Bach, Braun, Formella.. (1997) (Correct) (5 citations)
May 1996. 18] J. Keller. Fast rehashing in PRAM **emulations**. In Proc. of the 5th IEEE Symposium on Parallel
its local memory, the registers of the control **FPGA**, on-board I/O devices (two SCSI controllers, a
host. Particularly, some special registers of the **FPGA** controlling the state of the board may be set
www-wjp.cs.uni-sb.de/~lsbib/papers/PRAM/hiccs-pram.ps.gz

Heap Management in Hardware - Mavroidis (1998) (Correct) (1 citation)
possible hardware organizations of a heap using one **FPGA** and external memory. We also describe the
report focuses on the H/W implementation using one **FPGA** and external memory, which, with low cost, can
possible hardware organizations of a heap using one **FPGA** and external memory. We discuss the different
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An Effective Design System for Dynamically Reconfigurable.. - Sriram Govindarajan (Correct) (2 citations)
Computer (rc) that consists of a multi-**fpga** board with memory banks and interconnection
(SynthePre -Processor Bitmap files HOST Multi-**FPGA** Board Synthesis Logic/Layout Schedule
Micro Systems Inc.consists of four Xilinx XC4013 **fpgas** having 576 clbs each and four 32K memory banks
www.ece.uc.edu/~sriram/papers/fccm98.ps

Hardware Software Tri-Design Of Encryption For Mobile.. - Mencer, Morf, Flynn (Correct) (11 citations)
the design space of Field Programmable Gate Arrays (**FPGAs**)Processors and ASICs -Hardware-Software
MOPS/Watt and Mbits/s/Watt to compare processors, **FPGAs** and ASICs. We compare the latest Digital Signal
from Texas Instruments to Xilinx XC4000 series **FPGAs**. Many DSP-like applications perform very well on
umunhum.stanford.edu/oskar/icas98.ps

An Evaluation of Bipartitioning Techniques - Scott Hauck (1995) (Correct) (29 citations)
custom ASICs. Now, with the increasing use of **FPGA**-based emulators and prototyping systems,
been biased by the fact that we are targeting multi-**FPGA** systems. One part of this is that the time it
the final implementation. In contrast, a multi-**FPGA** system is ready to use seconds after the mapping
www.cs.washington.edu/research/lis/papers/postscript/hauck-Bipartition.ps

An Improved Algorithm for Performance Optimal Technology Mapping .. - Cong, Wu (1996) (Correct)

(3 citations)
Technology Mapping with Retiming in LUT-Based **FPGA** Design Jason Cong and Chang Wu Department of
of California, Los Angeles, CA 90024 Abstract The **FPGA** technology mapping and synthesis problem for
circuits with n gates and targeting K-LUT based **FPGAs**, which is too high for medium and large size
ftp.cs.ucla.edu/tech-report/96-reports/960012.ps.Z

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on a field programmable gate array, or **FPGA. FPGA**'s have proven extremely valuable in our design
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per second at 33 MHz PCI clock speed. With current **FPGA** technology the throughput would scale up easily to
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and Address Joint Highway Research Project **1284** Civil Engineering Building Purdue University West
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12 bit A/D converter, optical isolation and IEEE **1284** compatible fast bi-directional parallel interface
www.um.savba.sk/lab_21/files/ice98.ps.gz

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School of Civil Engineering, Purdue University, **1284** Civil Engineering Building, West Lafayette, IN
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Examples of External Interfaces - Below Some Potential (2000) (Correct)
Industry Standard) EPP Enhanced Parallel Port IEEE **1284** -connector with 25 or 36 wires Up to 1,5 Mbps
www.arib.or.jp/IMT-2000/ARIB-STD_V120Sep_00/DS-CDMA/TR-T12/27_series/27901-300.pdf

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